

WHAT IS CLAIMED IS:

- 1 1. A semiconductor device, comprising:
2 a plurality of circuit sections;
3 a plurality of local current generator (LCG), each LCG being coupled to at least one of
4 the circuit sections; and
5 a global reference current generator (GRCG), each LCG being coupled to the GRCG
6 through a plurality of conductive lines, wherein the resistance of the conductive lines between
7 each LCG and the GRCG is substantially the same.
- 1 2. The memory device according to Claim 1, wherein the length of the conductive lines
2 between each LCG and the GRCG is substantially the same.
- 1 3. The memory device according to Claim 1, wherein a reference current sent from the
2 GRCG to the plurality of LCGs is substantially the same at an input of each LCG.
- 1 4. The memory device according to Claim 1, wherein the plurality of conductive lines
2 comprises a first segment, a second segment coupled to the first segment, and a third segment
3 coupled to the first segment and second segment, wherein the plurality of LCGs comprises a first
4 LCG and a second LCG, wherein the first segment and the second segment are coupled between
5 the first LCG and the GRCG, wherein the first segment and the third segment are coupled
6 between the second LCG and the GRCG, and wherein the resistance of second segment and third
7 segment are substantially equal.

1 5. The memory device according to Claim 4, wherein the length of the second segment is
2 substantially equal to the length of the third segment.

1 6. The memory device according to Claim 1, wherein the sub-arrays comprise a plurality of
2 magnetic memory cells, wherein the memory device comprises a magnetic random access
3 memory (MRAM) device.

1 7. The memory device according to Claim 1, wherein the plurality of conductive lines are
2 formed in a single material layer of the memory device.

1 8. The memory device according to Claim 1, wherein the plurality of conductive lines are
2 formed in a plurality of material layers of the memory device.

1 9. The memory device according to Claim 1, wherein the plurality of conductive lines
2 comprise copper, aluminum or combinations thereof.

1 10. The memory device according to Claim 1, wherein the LCGs are arranged in columns or
2 rows.

1 11. A magnetic random access memory (MRAM) device, comprising;
2 a plurality of sub-arrays, each sub-array comprising:
3 a plurality of magnetic memory cells;
4 a plurality of first conductive lines disposed beneath the magnetic memory cells,
5 the first conductive lines being positioned in a first direction; and
6 a plurality of second conductive lines disposed above the magnetic memory cells,
7 the second conductive lines being positioned in a second direction;
8 a local current generator (LCG) coupled to each sub-array; and
9 a global reference current generator (GRCG) coupled to each local current generator
10 through a plurality of third conductive lines, wherein the resistance of the third conductive lines
11 between each LCG and the GRCG is substantially the same.

1 12. The MRAM device according to Claim 11, wherein the length of the third conductive
2 lines between each LCG and the GRCG is substantially the same.

1 13. The MRAM device according to Claim 11, wherein a reference current sent from the
2 GRCG to the plurality of LCGs is substantially the same at an input of each LCG.

1 14. The MRAM device according to Claim 11, wherein the plurality of third conductive lines
2 comprises a first segment, a second segment coupled to the first segment, and a third segment
3 coupled to the first segment and second segment, wherein the plurality of LCGs comprises a first
4 LCG and a second LCG, wherein the first segment and the second segment are coupled between
5 the first LCG and the GR CG, wherein first segment and the third segment are coupled between
6 the LCG and the GR CG, and wherein the resistance of the second segment and the third segment
7 are substantially equal.

1 15. The MRAM device according to Claim 14, wherein a first write current generated by the
2 first LCG is substantially equal to a second write current generated by the second LCG.

1 16. The MRAM device according to Claim 14, wherein the length of the second segment is
2 substantially equal to the length of the third segment.

1 17. The MRAM device according to Claim 11, wherein the plurality of third conductive lines
2 are formed in a single material layer of the MRAM device.

1 18. The MRAM device according to Claim 11, wherein the plurality of third conductive lines
2 are formed in a plurality of material layers of the MRAM device.

1 19. The MRAM device according to Claim 11, wherein the plurality of third conductive lines
2 comprise copper, aluminum or combinations thereof.

1 20. The MRAM device according to Claim 11, wherein the LCGs are arranged in columns or
2 rows.

1 21. In a semiconductor memory device comprising a plurality of local current generator
2 (LCGs) coupled to a global reference current generator (GRCG), a method of distributing current
3 comprises:

4 flowing current through a first current path from the GRCG to a first LCG; and
5 flowing current through a second current path from the GRCG to a second LCG, the
6 second current path having the same resistance as the first current path.

1 22. The method according to Claim 21, wherein the second current path has the same length
2 as the first current path.

1 23. The method according to Claim 21, further comprising:
2 flowing current through a third current path from the GRCG to a third LRCG circuit, the
3 third current path having the same resistance as the first and second current paths; and
4 flowing current through a fourth current path from the GRCG to a fourth LRCG circuit,
5 the fourth current path having the same resistance as the first, second and third current paths.

1 24. The method according to Claim 23, wherein the second current path, the third current
2 path and the fourth current path have the same length as the first current path.

1 25. The method according to Claim 23, wherein the first and second current paths are
2 coupled at a first point, and wherein the third and fourth current paths are coupled at a second
3 point.

1 26. The method according to Claim 25, wherein the first and second current paths are
2 coupled with the third and fourth current paths at a third point.

1 27. The method according to Claim 21, wherein the first and second current paths are
2 coupled at a first point.